Edidi Sai Anant

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OBJECTIVE

Electrical Engineering Master's candidate with a robust foundation in semiconductor processes and IC design, built on a comprehensive academic background and hands-on experience. Keen on exploring diverse opportunities within the Semiconductor industry to further enhance and apply this foundational knowledge. Driven by a passion for innovation and equipped with analytical and technical skills, committed to contributing to collaborative teams and embracing challenges in a dynamic, future-oriented environment.
Strength: Reliable, Patient, and a Collaborative Team Player

EDUCATION

National University of Singapore, *Master of Science Electrical Engineering* 08/2023 – 06/2025
Singapore

Relevant Courses:
- VLSI Digital Circuit Design
- Memory Technologies and Their Emerging Applications
- Embedded Hardware System Design

Graduate Assistant:
- Oversaw laboratory sessions and assisted with assignments and grading for:
  - EE2028 Microcontroller Programming and Interfacing
  - CG3207 Computer Architecture
- Provided guidance and feedback on lab work.
- Collaborated with faculty to overhaul lab materials and processes.

SRM Institute of Science and Technology, 06/2019 – 07/2023
Bachelor of Technology Electronics and Communication Engineering Chennai, India

Relevant Courses:
- Digital Electronics Principles
- Semiconductor Device Modelling
- Analog Electronic Circuits
- Microprocessor, Microcontroller and Interfacing Techniques
- Analog and Digital Communication
- VLSI Design
- ARM- Based Embedded System Design

INTERNSHIP EXPERIENCE

Maven Silicon, *Project Intern* 12/2022 – 01/2023
Banglore, India

- Developed expertise in analysing project requirements to establish clear and efficient development plans.
- Designed an AHB to APB bridge, tailoring it to meet specific project needs and facilitating seamless communication between distinct bus protocols.
- Decomposed complex designs into modular components, increasing manageability and design efficiency.
- Executed module-level design, honing the ability to realise projects from concept to completion with a keen attention to detail.
- Advanced proficiency in writing robust, functional RTL code in Verilog HDL, ensuring optimal performance.
- Interpreted RTL descriptions into gate-level schematics and refining design for efficiency and reliability.
- Synthesized individual modules into a unified, top-tier system architecture, ensuring cohesive operation and performance.

Sandeepani School of Embedded System Design, *Intern* 06/2022 – 07/2022
Banglore, India

- Collaborated on the development and meticulous verification of a UART protocol using Verilog HDL, concentrating on data transmission reliability and system integrity.
- Executed in-depth functional verification of a Half Adder utilising SystemVerilog, ensuring alignment with precise performance specifications.
- Performed detailed functional coverage analysis employing QuestaSim, aiming for exhaustive assessment and optimisation of test scenarios.

PUBLICATIONS

Improving Data Integrity with Reversible Logic-based Error Detection and Correction Module on AHB-APB Bridge, *IEEE* 05/2023

A Survey on Affordable Internet of Things (IoT) Enabled Healthcare Systems, 06/2022
Grenze International Journal of Engineering and Technology

PROJECTS

VLSI Interconnect Modelling and Simulation

Engaged in optimising processor interconnects using Elmore RC models and Cadence Virtuoso for a 2-core processor at 45nm technology, focusing on energy-delay tradeoffs to improve system efficiency. Combined theory with practice to address VLSI design challenges, improving signal integrity and system performance.

Digital Circuit Design and Standard Cell IP Development

Contributed to the creation of a ring oscillator Standard Cell IP leveraging a hierarchical design in Cadence Virtuoso, targeting efficiency in 40nm technology with a focus on minimising area while optimising PVT. Ensured design integrity through strict adherence to DRC and LVS standards.

FPGA Hardware Accelerator for MLP Neural Network

Developed a hardware accelerator on the Xilinx Zynq-7000 FPGA to improve MLP neural network inference. Implemented designs in software, HLS, and Verilog, focusing on prediction. Executed profiling and optimisation utilising pipelining, loop unrolling, and array partitioning, achieving significant speed and efficiency gains.

In-Memory Compute Circuit for Neural Network Acceleration

Designed an in-memory compute circuit using NeuroSim and MuMax3 to accelerate neural network computations. Concentrated on quantization and optimisation techniques to boost accuracy and efficiency. Conducted simulations in PyTorch, comparing different data types (float64, float32, int8, int4) to analyse model performance. Implemented profiling and optimisation strategies, achieving significant improvements in computational speed and resource utilisation.

CERTIFICATIONS

Introduction to IoT and Digital Transformation, *Cisco Networking Academy*

Python for Data Science, AI & Development, *Coursera and IBM*

Introduction to Programming in C++, *edX and NYU*

PCB Design, *Internshala Training*

Business Considerations for 5G with Edge, IoT, and AI, *edX and The Linux Foundation*

IoT Systems and Industrial Applications with Design Thinking, *edX and EPFL*

Programming for Everybody (Getting Started with Python), *Coursera and University of Michigan*

Building a RISC-V CPU Core, *edX and The Linux Foundation*

Embedded Systems Essentials with Arm: Getting Started, *edX and ARM Education*

TECHNICAL SKILLS

Embedded Systems: Arduino • NodeMCU • Raspberry Pi | **EDA Tools:** Cadence Virtuoso • Xilinx Vivado • QuestaSim • Xilinx Vitis | **Programming:** C++ • Python | **PCB Design:** Autodesk Eagle | **HDL:** Verilog • SystemVerilog • HLS | **LaTeX**

SOFT SKILLS

Congenial and Focused
Collaboration and Teamwork
Multitasking and Prioritisation
Empathetic and Compassionate

INTERESTS

Solving Puzzles | Listening to music | Playing video games | Travelling | Cooking